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ART UNIT	PAPER NUMBER
2133	6

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/975,293	YEUNG ET AL.	
	Examiner	Art Unit	
	Joseph D. Torres	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 April 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings were received on 15 April 2004. These drawings are accepted.

Claim Rejections - 35 USC § 112 of Previous Office Action

2. In view of Amendment A in Paper No. 4, the Examiner withdraws all previous 35 USC § 112 rejections to the claims.

Response to Amendment

3. Applicant's arguments with respect to claims 1-21 have been considered but are moot in view of the new ground(s) of rejection. Note: Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-6, 8, 11, 14-20 and 22 are rejected under 35 U.S.C. 102(b) as being anticipated by Stiffler; Jack J. (US 4736376 A).

35 U.S.C. 102(b) rejection of claim 1.

Stiffler teaches an apparatus for memory error control coding (col. 1, lines 11-20 in Stiffler teach that the error control coding taught in the Stiffler patent is directed to system memory storage units) comprising a first circuit configured to generate a first syndrome signal in response to a read data signal and a read parity signal (Table I in col. 19 of Stiffler teaches that 1st Stage Syndrome Generator 430 in Figure 4 of Stiffler is employed in response to data read; Note: since data is encoded, the encoded data comprises a read data signal and a read parity signal, which the 1st Stage Syndrome Generator 430 responds to by producing first syndrome signals; Note also; 1st Stage Syndrome Generator 430 in each half of the decoder in Figure 3 of Stiffler produces signals [c1...c4] and [e1...e4], hence signals [c1...c4] and [e1...e4] are first syndrome signals corresponding to the first half of the decoder in Figure 3; in particular, the two sets of [c1...c4] for both decoders in Figure 3 is a first syndrome signal, and [e1...e4] for both decoders in Figure 3 is another first syndrome signal; Note: For the purposes of this rejection the two sets of [c1...c4] for each decoder comprise the first syndrome signal); a bypass circuit configured to generate a second syndrome signal in response to said first syndrome signal and a bypass signal (the 2nd Stage Syndrome Generators 442 and 444 in Figure 4 of Stiffler comprise a bypass circuit configured to generate half of second syndrome signals [h1...h4] and [i1...i4] for each decoder in Figure 3 in response to said first syndrome signals [c1...c4] and [e1...e4] and a bypass signal [g1...g4], hence the bypass circuit, 2nd Stage Syndrome Generators 442 and 444 of

both decoders in Figure 3, is configured to generate second syndrome signals comprising [h1...h4] and [i1...i4] in the first and second decoders in response to said first syndrome signal [c1...c4] and a bypass signal from Encoder/Decoder Control 420; Note: For the purposes of this rejection the two sets of [h1...h4] for each decoder comprise the second syndrome signal; Note also that 2nd Stage Syndrome Generators 442 and 444 are bypassed during encoding, hence are responsive to the bypass signal generated by Encoder/Decoder Control 420); and a second circuit configured to i. detect an error when said bits of said second syndrome signal are not all the same state and ii. generate an error location signal [j1...j4] in response to said second syndrome signal [h1...h4], wherein said error location signal [j1...j4] is generated in response to fewer than all of said bits of said second syndrome signal (col. 9, lines 28-30 in Stiffler teach that if some of the syndrome values in the second syndrome signal [h1...h4] are non-zero then an error is detected and the error location signal [j1...j4] is produced; Note: Only half of the second syndrome signal [h1...h4] corresponding to a single decoder are used to produce each set of error location signals [j1...j4], hence the error location signal [j1...j4] is generated in response to fewer than all of said bits of said second syndrome signal [h1...h4], hence 1st Stage Syndrome Decoder 458 is a second circuit configured to i. detect an error when said bits of said second syndrome signal are not all the same state and ii. generate an error location signal [j1...j4] in response to said second syndrome signal [h1...h4], wherein said error location signal [j1...j4] is generated in response to fewer than all of said bits of said second syndrome signal).

35 U.S.C. 102(b) rejection of claim 2.

Stiffler teaches all of said bits of said first syndrome signal are at a particular state when no error is detected in said read data and parity signals and said particular state comprises a digital 1 (col. 9, lines 52-55 in Stiffler teach that d1="1" or d2="1" indicates an error; col. 12, lines 59-61 in Stiffler teach that [c1...c4] are all "true"="1" when d1="0" and d2="1" indicating an error).

35 U.S.C. 102(b) rejection of claim 3.

Stiffler teaches said apparatus is configured to present said read data and parity signals at an output when no error is detected in said read data and parity signals (Note: Byte Parity Corrector 498 and Valid Data bit Generator 497 in Figure 4 of Stiffler present said read data and parity signals at an output whether no error is detected or not in said read data and parity signals).

35 U.S.C. 102(b) rejection of claim 4.

The circuit in Figure 4 of Stiffler is substantially a memory circuit configured to receive a data input signal and a parity signal and present said read data and parity signals during a read operation (see rejection to claim 1 for details on the operation of the memory circuit in Figure 4 of Stiffler).

35 U.S.C. 102(b) rejection of claim 5.

Stiffler teaches said second circuit is configured to generate a single error signal when a

single bit error is detected in said read data and parity signals (col. 6, line 65-68 in Stiffler teaches an interrupt signal is generated in the case of a correctable error; Note: a correctable error is a single bit error in Stiffler, hence the interrupt signal is a single error signal), a double error signal when an error is detected in two bits of said read data and parity signals (col. 17, lines 58-60 in Stiffler teaches that Gate 1620 in Figure 16 will produce a "low" output signal if an uncorrectable error situation occurs; Note: an uncorrectable error is a double error in Stiffler, hence the "low" output signal is a double error signal), and an error detected signal when either said single error signal or said double error signal are generated in response to said second syndrome signal (col. 10, lines 14-16 in Stiffler teaches that q1 and q2 are error detected signals).

35 U.S.C. 102(b) rejection of claim 6.

Stiffler teaches said apparatus is configured to generate a corrected representation of said read data and parity signals when a single bit error is detected (Data Corrector 488, Byte Parity Corrector 490 and Valid Data Bit Generator 491 in Figure 4 of Stiffler all produce corrected data and parity signals in response to a correctable error).

35 U.S.C. 102(b) rejection of claim 8.

Figure 8 in Stiffler teaches second syndrome signal [h1...h4] is produced using non-inverting exclusive-Or gates, which is a type selected from the group consisting of (i) **non-inverting exclusive-OR gates**, (ii) non-inverting exclusive-OR gates with an output inverted by a NOT gate, (iii) inverting exclusive-OR gates, (iv) inverting

exclusive-OR gates with an output inverted by a NOT gate, (v) non-inverting exclusive-NOR gates, (vi) inverting exclusive-NOR gates, (vii) non-inverting exclusive-NOR gates with an output inverted by a NOT gate, and (viii) inverting exclusive-NOR gates with an output inverted by a NOT gate.

35 U.S.C. 102(b) rejection of claim 11.

Figure 7 in Stiffler teaches first syndrome signal [c1...c4] is produced using non-inverting exclusive-Or gates and non-inverting exclusive-Or gates with an output inverted by a NOT gate, which is a type selected from the group consisting of (i) non-inverting exclusive-OR gates, (ii) **non-inverting exclusive-OR gates with an output inverted by a NOT gate**, (iii) **inverting exclusive-OR gates**, (iv) inverting exclusive-OR gates with an output inverted by a NOT gate, (v) non-inverting exclusive-NOR gates, (vi) inverting exclusive-NOR gates, (vii) non-inverting exclusive-NOR gates with an output inverted by a NOT gate, and (viii) inverting exclusive-NOR gates with an output inverted by a NOT gate. Note: Figure 7 in Stiffler teaches first syndrome signal [e1...e4] is produced using non-inverting exclusive-Or gates and non-inverting exclusive-Or gates with an output inverted by a NOT gate, which is a type selected from the group consisting of (i) **non-inverting exclusive-OR gates**, (ii) **non-inverting exclusive-OR gates with an output inverted by a NOT gate**, (iii) inverting exclusive-OR gates, (iv) inverting exclusive-OR gates with an output inverted by a NOT gate, (v) non-inverting exclusive-NOR gates, (vi) inverting exclusive-NOR gates, (vii) non-inverting exclusive-NOR gates with an output inverted by

a NOT gate, and (viii) inverting exclusive-NOR gates with an output inverted by a NOT gate.

35 U.S.C. 102(b) rejection of claim 14.

Stiffler teaches an apparatus for memory error control coding coding (col. 1, lines 11-20 in Stiffler teach that the error control coding taught in the Stiffler patent is directed to system memory storage units) comprising: means for generating a first syndrome signal in response to a read data signal and a read parity signal (Table I in col. 19 of Stiffler teaches that 1st Stage Syndrome Generator 430 in Figure 4 of Stiffler is employed in response to data read; Note: since data is encoded, the encoded data comprises a read data signal and a read parity signal, which the 1st Stage Syndrome Generator 430 responds to by producing first syndrome signals; Note also; 1st Stage Syndrome Generator 430 in each half of the decoder in Figure 3 of Stiffler produces signals [c1...c4] and [e1...e4], hence signals [c1...c4] and [e1...e4] are first syndrome signals corresponding to the first half of the decoder in Figure 3; in particular, the two sets of [c1...c4] for both decoders in Figure 3 is a first syndrome signal, and [e1...e4] for both decoders in Figure 3 is another first syndrome signal; Note: For the purposes of this rejection the two sets of [c1...c4] for each decoder comprise the first syndrome signal); means for generating a second syndrome signal in response to said first syndrome signal and a bypass signal (the 2nd Stage Syndrome Generators 442 and 444 in Figure 4 of Stiffler comprise a bypass circuit configured to generate half of second syndrome signals [h1...h4] and [i1...i4] for each decoder in Figure 3 in response to said first

syndrome signals [c1...c4] and [e1...e4] and a bypass signal [g1...g4], hence the bypass circuit, 2nd Stage Syndrome Generators 442 and 444 of both decoders in Figure 3, is configured to generate second syndrome signals comprising [h1...h4] and [i1...i4] in the first and second decoders in response to said first syndrome signal [c1...c4] and a bypass signal from Encoder/Decoder Control 420; Note: For the purposes of this rejection the two sets of [h1...h4] for each decoder comprise the second syndrome signal; Note also that 2nd Stage Syndrome Generators 442 and 444 are bypassed during encoding, hence are responsive to the bypass signal generated by Encoder/Decoder Control 420); and means for detecting an error when said bits of said second syndrome signal are not all the same state and generating an error location signal in response to said second syndrome signal, wherein said error location signal is generated in response to fewer than all of said bits of said second syndrome signal (col. 9, lines 28-30 in Stiffler teach that if some of the syndrome values in the second syndrome signal [h1...h4] are non-zero then an error is detected and the error location signal [j1...j4] is produced; Note: Only half of the second syndrome signal [h1...h4] corresponding to a single decoder are used to produce each set of error location signals [j1...j4], hence the error location signal [j1...j4] is generated in response to fewer than all of said bits of said second syndrome signal [h1...h4], hence 1st Stage Syndrome Decoder 458 is a second circuit configured to i. detect an error when said bits of said second syndrome signal are not all the same state and ii. generate an error location signal [j1...j4] in response to said second syndrome signal [h1...h4], wherein said error location signal [j1...j4] is generated in response to fewer than all of said bits of said

second syndrome signal).

35 U.S.C. 102(b) rejection of claim 15.

Stiffler teaches a method for memory error detection and correction (col. 1, lines 11-20 in Stiffler teach that the error control coding taught in the Stiffler patent is directed to system memory storage units and a method for using the device) comprising the steps of generating a first syndrome signal in response to a read data signal and a read parity signal (Table I in col. 19 of Stiffler teaches that 1st Stage Syndrome Generator 430 in Figure 4 of Stiffler is employed in response to data read; Note: since data is encoded, the encoded data comprises a read data signal and a read parity signal, which the 1st Stage Syndrome Generator 430 responds to by producing first syndrome signals; Note also; 1st Stage Syndrome Generator 430 in each half of the decoder in Figure 3 of Stiffler produces signals [c1...c4] and [e1...e4], hence signals [c1...c4] and [e1...e4] are first syndrome signals corresponding to the first half of the decoder in Figure 3; in particular, the two sets of [c1...c4] for both decoders in Figure 3 is a first syndrome signal, and [e1...e4] for both decoders in Figure 3 is another first syndrome signal; Note: For the purposes of this rejection the two sets of [c1...c4] for each decoder comprise the first syndrome signal); generating a second syndrome signal in response to said first syndrome signal and a bypass signal (the 2nd Stage Syndrome Generators 442 and 444 in Figure 4 of Stiffler comprise a bypass circuit configured to generate half of second syndrome signals [h1...h4] and [i1...i4] for each decoder in Figure 3 in response to said first syndrome signals [c1...c4] and [e1...e4] and a bypass signal

[g1...g4], hence the bypass circuit, 2nd Stage Syndrome Generators 442 and 444 of both decoders in Figure 3, is configured to generate second syndrome signals comprising [h1...h4] and [i1...i4] in the first and second decoders in response to said first syndrome signal [c1...c4] and a bypass signal from Encoder/Decoder Control 420; Note: For the purposes of this rejection the two sets of [h1...h4] for each decoder comprise the second syndrome signal; Note also that 2nd Stage Syndrome Generators 442 and 444 are bypassed during encoding, hence are responsive to the bypass signal generated by Encoder/Decoder Control 420); detecting an error when said bits of said second syndrome signal are not all the same state; and generating an error location signal in response to said second syndrome signal, wherein said error location signal is generated in response to fewer than all of said bits of said second syndrome signal (col. 9, lines 28-30 in Stiffler teach that if some of the syndrome values in the second syndrome signal [h1...h4] are non-zero then an error is detected and the error location signal [j1...j4] is produced; Note: Only half of the second syndrome signal [h1...h4] corresponding to a single decoder are used to produce each set of error location signals [j1...j4], hence the error location signal [j1...j4] is generated in response to fewer than all of said bits of said second syndrome signal [h1...h4], hence 1st Stage Syndrome Decoder 458 is a second circuit configured to i. detect an error when said bits of said second syndrome signal are not all the same state and ii. generate an error location signal [j1...j4] in response to said second syndrome signal [h1...h4], wherein said error location signal [j1...j4] is generated in response to fewer than all of said bits of said second syndrome signal).

35 U.S.C. 102(b) rejection of claim 16.

Stiffler teaches all of said bits of said first syndrome signal are at a particular state when no error is detected in said read data and parity signals and said particular state comprises a digital 1 (col. 9, lines 52-55 in Stiffler teach that d1="1" or d2="1" indicates an error; col. 12, lines 59-61 in Stiffler teach that [c1...c4] are all "true"="1" when d1="0" and d2="1" indicating an error).

35 U.S.C. 102(b) rejection of claim 17.

Stiffler teaches bypassing said error location signal generating sub step step in response to a predetermined state of said bypass signal (during encoding, i.e., the bypass signal from Encoder/Decoder Control 420 is in a second state, error correction is disabled).

35 U.S.C. 102(b) rejection of claim 18.

Stiffler teaches said second circuit is configured to generate a single error signal when a single bit error is detected in said read data and parity signals (col. 6, line 65-68 in Stiffler teaches an interrupt signal is generated in the case of a correctable error; Note: a correctable error is a single bit error in Stiffler, hence the interrupt signal is a single error signal), a double error signal when an error is detected in two bits of said read data and parity signals (col. 17, lines 58-60 in Stiffler teaches that Gate 1620 in Figure 16 will produce a "low" output signal if an uncorrectable error situation occurs; Note: an

uncorrectable error is a double error in Stiffler, hence the "low" output signal is a double error signal), and an error detected signal when either said single error signal or said double error signal are generated in response to said second syndrome signal (col. 10, lines 14-16 in Stiffler teaches that q1 and q2 are error detected signals).

35 U.S.C. 102(b) rejection of claim 19.

Stiffler teaches said apparatus is configured to present said read data and parity signals at an output when no error is detected in said read data and parity signals (Note: Byte Parity Corrector 498 and Valid Data bit Generator 497 in Figure 4 of Stiffler present said read data and parity signals at an output whether no error is detected or not in said read data and parity signals).

35 U.S.C. 102(b) rejection of claim 20.

Stiffler teaches said apparatus is configured to generate a corrected representation of said read data and parity signals when a single bit error is detected (Data Corrector 488, Byte Parity Corrector 490 and Valid Data Bit Generator 491 in Figure 4 of Stiffler all produce corrected data and parity signals in response to a correctable error).

35 U.S.C. 102(b) rejection of claim 22.

Stiffler teaches an apparatus for memory error control coding (col. 1, lines 11-20 in Stiffler teach that the error control coding taught in the Stiffler patent is directed to system memory storage units and a method for using the device) comprising:

a syndrome encoder circuit configured to generate a syndrome signal in response to a read data signal and a read parity signal, wherein said syndrome encoder circuit comprises a type of syndrome encoder selected from the group consisting of i. non-inverting exclusive-OR gates with an output inverted by a NOT gate, ii. inverting exclusive-OR gates, iii. inverting exclusive-OR gates with an output inverted by a NOT gate, iv. non-inverting exclusive-NOR gates, v. non--inverting exclusive-NOR gates with an output inverted by a NOT gate, vi. inverting exclusive-NOR gates, and vii. inverting exclusive-NOR gates with an output inverted by a NOT gate (Figure 7 in Stiffler teaches first syndrome signal [c1...c4] is produced using non-inverting exclusive-Or gates and non-inverting exclusive-Or gates with an output inverted by a NOT gate, which is a type selected from the group consisting of i. non-inverting exclusive-OR gates, ii. **non-inverting exclusive-OR gates with an output inverted by a NOT gate**, iii. **inverting exclusive-OR gates**, iv. inverting exclusive-OR gates with an output inverted by a NOT gate, v. non-inverting exclusive-NOR gates, vi. inverting exclusive-NOR gates, vii. non-inverting exclusive-NOR gates with an output inverted by a NOT gate, and viii. inverting exclusive-NOR gates with an output inverted by a NOT gate; Figure 7 in Stiffler teaches first syndrome signal [e1...e4] is produced using non-inverting exclusive-Or gates and non-inverting exclusive-Or gates with an output inverted by a NOT gate, which is a type selected from the group consisting of i. **non-inverting exclusive-OR gates**, ii. **non-inverting exclusive-OR gates with an output inverted by a NOT gate**, iii. inverting exclusive-OR gates, iv. inverting exclusive-OR gates with an output inverted by a NOT gate, v. non-inverting exclusive-NOR gates, vi. inverting

exclusive-NOR gates, vii. non-inverting exclusive-NOR gates with an output inverted by a NOT gate, and viii. inverting exclusive-NOR gates with an output inverted by a NOT gate); and a second circuit configured to i. detect an error when bits of said syndrome signal are not all the same state and ii. generate an error location signal in response to said syndrome signal, wherein said error location signal is generated in response to fewer than all of said bits of said syndrome signal (col. 9, lines 28-30 in Stiffler teach that if some of the syndrome values in the second syndrome signal [h1...h4] are non-zero then an error is detected and the error location signal [j1...j4] is produced; Note: Only half of the second syndrome signal [h1...h4] corresponding to a single decoder are used to produce each set of error location signals [j1...j4], hence the error location signal [j1...j4] is generated in response to fewer than all of said bits of said second syndrome signal [h1...h4], hence 1st Stage Syndrome Decoder 458 is a second circuit configured to i. detect an error when said bits of said second syndrome signal are not all the same state and ii. generate an error location signal [j1...j4] in response to said second syndrome signal [h1...h4], wherein said error location signal [j1...j4] is generated in response to fewer than all of said bits of said second syndrome signal).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 7, 9, 10, 12, 13, 21 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stiffler; Jack J. (US 4736376 A).

35 U.S.C. 103(a) rejection of claim 7.

Stiffler substantially teaches the claimed invention described in claims 1-6 (as rejected above). In addition, col. 10, lines 6-8 in Stiffler teach the 2nd Stage Syndrome Generator 444 in Figure 4 of Stiffler produces the inverse half [i1…i4] of the second syndrome bits [h1…h4].

However Stiffler does not explicitly teach the specific use of inverting each of said bits of said second syndrome signal **in the second circuit**.

The Examiner asserts that Figure 4 of Stiffler is a block diagram for establishing the logical layout of the design and that the actual circuit layout is based on obvious engineering design choices, hence an embodiment of the design in the Stiffler patent including 2nd Stage Syndrome Generator 444 in Figure 4 as part of the second circuit, 1st Stage Syndrome Decoder 458, is an obvious engineering design choice based on

actual design requirements such as cost, feasibility, available space, stray capacitance, etc.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Stiffler by including 2nd Stage Syndrome Generator 444 in Figure 4 of Stiffler as part of the second circuit, 1st Stage Syndrome Decoder 458. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that including 2nd Stage Syndrome Generator 444 in Figure 4 as part of the second circuit, 1st Stage Syndrome Decoder 458 would have provided the opportunity to implement an embodiment of the circuit in Figure 4 of Stiffler based on obvious engineering design choice such as cost, feasibility, available space, stray capacitance, etc.

35 U.S.C. 103(a) rejection of claims 9 and 23.

Stiffler substantially teaches the claimed invention described in claims 1-9 (as rejected above). In addition, Stiffler teaches one or more OR gates (930, 936, 942 & 948 in Figure 9 and 1506 & 1510 in Figure 15 of Stiffler) configured to receive an inverse ([i1…i4] in Figure 9) of said second syndrome signal ([h1…h4] in Figure 9) and present said error detected signal (q1 and q2); one or more exclusive-OR gates configured to receive an inverse of said second syndrome signal and present an intermediate signal (col. 15, lines 23-43 in Stiffler teach that exclusive-OR gates 1202-1208 are configured to receive an inverse [i1…i4] of said second syndrome signal and present an

intermediate signal [s1...s4]); one or more AND gates configured to present said single error signal in response to said error detected signal and said intermediate signal (intermediate signal [s1...s4] comprise parity for a stored word and are stored with the word in memory and upon reading the word are submitted to the decoder via 401 whereby [s1...s4]=[b17=b20]; Note: [b17=b20] are used to generate [c1...c4] and [e1...e4] in Figure 7, which are used to generate [h1...h4] and [i1...i4] in Figure 8 which are submitted to one or more AND gates 926-980 in Figure 9 to produce [j1...j4] and [l1...l4] which are used to produce said single error signal and said double error signal); and an AND gate configured to present said double error signal in response to said error detected signal and said intermediate signal (intermediate signal [s1...s4] comprise parity for a stored word and are stored with the word in memory and upon reading the word are submitted to the decoder via 401 whereby [s1...s4]=[b17=b20]; Note: [b17=b20] are used to generate [c1...c4] and [e1...e4] in Figure 7, which are used to generate [h1...h4] and [i1...i4] in Figure 8 which are submitted to one or more AND gates 926-980 in Figure 9 to produce [j1...j4] and [l1...l4] which are used to produce said single error signal and said double error signal; Note: NAND gates 902-918 substantially invert output which is equivalent to ORing the inverse of the inputs). However Stiffler does not explicitly teach the specific use of an AND gate configured to present said double error signal in response to said error detected signal and **an inverse** of said intermediate signal (Note: Stiffler teaches an AND gate configured to present said double error signal in response to said error detected signal and said intermediate signal, see previous paragraph, above).

The Examiner asserts that NAND gates 902-918 in Figure 9 substantially invert output, which is equivalent to ORing the inverse of the inputs; hence use of an inverted intermediate signal is substantially an equivalent embodiment. One of ordinary skill in the art at the time the invention was made would have been highly motivated to invert the intermediate signal based on obvious engineering design choices such as available circuitry, design layout, and intrinsic qualities of circuit components that effect overall efficiency and cost of circuitry.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Stiffler by including use of an AND gate configured to present said double error signal in response to said error detected signal and **an inverse** of said intermediate signal. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of an AND gate configured to present said double error signal in response to said error detected signal and **an inverse** of said intermediate signal would have provided the opportunity to implement a substantially equivalent embodiment of the circuit of Figure 4 in Stiffler based on obvious engineering design choices such as available circuitry, design layout, and intrinsic qualities of circuit components that effect overall efficiency and cost of circuitry.

35 U.S.C. 103(a) rejection of claim 10.

Stiffler substantially teaches said single error signal comprises a multi-bit digital signal since the three bits, one each from NOR Gates 1620, 1436 and 1438 in Figures 14 and

16 are used to indicate correctable and uncorrectable errors, i.e., single and double errors.

35 U.S.C. 103(a) rejection of claim 12.

Stiffler substantially teaches the claimed invention described in claims 1-11 (as rejected above). In addition, Stiffler teaches said apparatus bypass circuit comprises one or more logic gates configured to receive said first syndrome signal (Figure 8 in Stiffler are one or more logic gates configured to receive said first syndrome signal [c1...c4]) wherein said first syndrome signal is presented as said second syndrome signal in response to said bypass signal having a first state (Figure 8 in Stiffler teaches that, during decoding, i.e., the bypass signal from Encoder/Decoder Control 420 is in a first state, said first syndrome signal [c1...c4] is substantially presented as said second syndrome signal [h1...h4] since the second syndrome signal is a modified version of the said first syndrome signal) and generation of said error location signal is disabled in response to said bypass signal having a second state (during encoding, i.e., the bypass signal from Encoder/Decoder Control 420 is in a second state, error correction is disabled).

However Stiffler does not explicitly teach the specific use of an apparatus bypass circuit comprising one or more logic gates configured to receive said bypass signal.

The Examiner asserts that 2nd Stage Syndrome Generators 442 and 444 Bypass circuits in Figure 4 of Stiffler are required to operate to transfer output data in two different modes, one mode during decoding and another mode during encoding, hence

although Stiffler does not explicitly teach that the 2nd Stage Syndrome Generators 442 and 444 receive the bypass signal from Encoder/Decoder Control 420, one of ordinary skill in the art at the time the invention was made would have recognized the need for notifying the 2nd Stage Syndrome Generators 442 and 444 in order to implement the design in the Stiffler patent.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to with the teachings of the Stiffler patent by including use of an apparatus bypass circuit comprising one or more logic gates configured to receive said bypass signal. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of said apparatus bypass circuit comprises one or more logic gates configured to receive said bypass signal would have provided the opportunity to implement the design in the Stiffler patent.

35 U.S.C. 103(a) rejection of claim 13.

Stiffler substantially teaches said one or more logic gates are selected from the group consisting of gates AND, NAND, NOR, and OR gates (See Figure 8 of Stiffler which teaches said one or more logic gates are OR gates, hence are selected from the group consisting of gates AND, NAND, NOR, and OR gates).

35 U.S.C. 103(a) rejection of claim 21.

Stiffler substantially teaches said bypass circuit is configured to present all of said bits of

said second syndrome signal having the same state in response to said bypass signal having said second state (during Encoding, i.e., the bypass signal from Encoder/Decoder Control 420 is in a second state, said second syndrome signal [h1...h4] and [i1...i4] is passed to Encoder 464: Note: if no errors occur the second syndrome signal is equal to zero).

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Lin, Shih-Chuan et al. (US 20020041647 A1) teaches a burst synchronization and error detection device and the method that is utilized in a communication system (such as the PACS system) using the time-division multiplexing/time division multiplex access (TDM/TDMA) technique.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a). A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (703) 308-7066. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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Art Unit 2133